



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,472	04/26/2002	Hideharu Ozaki	15483	1170

23389 7590 05/20/2005

SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

EXAMINER

KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
----------	--------------

2133

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/063,472

Applicant(s)

OZAKI, HIDEHARU

Examiner

JAMES C. KERVEROS

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 April 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
4a) Of the above claim(s) 5-20, 25-29, 31 and 33-36 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-4, 21-24, 30 and 32 is/are rejected.
7) ☒ Claim(s) 1-4, 21-24, 30 and 32 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 26 April 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a Non-Final Office Action in response to AMENDMENT and RCE filed 4/21/2005, which is in reply to the Final and Advisory Office Actions mailed 10/20/2004 and 3/22/2005.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/21/2005 has been entered.

Election/Restrictions

Claims 5-20, 25-29, 31 and 33-36 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse on 1/2/2004 of Species of Figure 7, readable on claims 1-4, 21-24, 30 and 32.

Claims 1-36 are still pending. Claims 1-4, 21-24, 30 and 32 are presently under examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy of JP 2001-229629, 07/30/2001, has been filed in parent Application No. 10/063,472, filed on 4/26/2002.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because of hand written notations and too small character size. Applicant is advised to employ the services of a competent patent draftsman outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Objections

Claims 1-4, 21-24, 30 and 32 are objected to because of the following informalities:

Claims 2-4, 21-24, 30 and 32 are objected to because the expression "A test circuit", recited on line 1 of the preamble of each claim, should be changed to "The test circuit", since it is the same test circuit as the test circuit of independent claim 1.

Claim 21, the expression "according to claim 1" should be deleted, because claim 21 cannot depend on claims 1 and 3.

Claim 1, on line 2, the term "therein" should be replaced by "in the semiconductor integrated circuit device", so as to clearer indicate the location of the scan-path test circuit. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2133

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 22 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "easily" recited in claims 22 and 23 is a relative term, which renders the claims indefinite. The term "easily" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The term "easily" does not provide a clear definition of a frequency measurement of the test clock, because the claimed invention does not provide a specific method or explanation of how to easily perform frequency measurements, since dividing the frequency of the test clock into a lower frequency does not necessarily result into easy frequency measurements.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Peng (U.S. Patent No. 5,524,114), issued: June 4, 1996.

Regarding independent Claim 1, Peng discloses, Figures 1, 2 and 3, a semiconductor die test jig 104 for holding and probing a semiconductor integrated circuit die or dice 202 having a test circuit including scan-path logic 214, VCO 204, phase detector 206, frequency divider 210, and burst controller 208 to enable scan-path delayed ATPG testing of the combinational logic 212, comprising:

A two-pulse generator (burst controller 208) for generating two clock pulses (310a and 310b) spaced from each other by a pulse interval equal to a period of a test clock (SCK-1) 222, which is originated from an external source (VCO 204), where the clock pulses 310a and 310b are applied as G-SCK-1 224 to the combinational logic 212 at time 318 which begins the scan-path data test of the combinational logic 212. The first clock pulse 310a causes the combinational logic 212 to start processing the scan-path data, and the second clock pulse 310b to stop the data processing,

Wherein the two-pulse generator (burst controller 208) comprises:

A gate signal generator, such as the burst controller 208 is utilized to "gate off and control the number of clock pulses to the combinational logic 212 during testing" (col. 6, lines 10-15), by gating signals CTL 112 and TCK 110 with SCK-1 222, Figure 3, the burst controller 208 allows only two clock pulses 310a and 310b to pass through. The clock pulses 310a and 310b are derived from the clock pulses 312 of the test clock SCK-1 222.

Regarding Claim 2, Peng discloses the test circuit of claim 1 is fabricated in the semiconductor integrated circuit die or dice 202 and further comprises:

A PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by $1/N$ (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is part of the test circuit, which is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3, 4, 21-24, 30 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peng (U.S. Patent No. 5,524,114) in view of Conner (U.S. Patent No. 5,794,175).

Regarding Claim 3, Pen substantially discloses the claimed invention as applied to claims 1 and 2 above. Peng does not explicitly disclose a test circuit mounted on a test board and a semiconductor integrated circuit device removably mounted on the test

board. However, Peng discloses a semiconductor die test jig 104, corresponding to a PCB test board, for holding and probing a semiconductor integrated circuit die or dice 202 having a test circuit, Figure 1 and 2. Furthermore, in analogous art, Conner discloses a printed circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuits, DUTs 116, for burn-in quality testing. The Memory array board 210 also includes a test fan out circuitry 214 that controls the provision of data from the devices under test 116 to error processor 124, (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets and a test circuit as taught by Conner on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the sockets for burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claim 4, Peng discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by $1/N$ (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Regarding Claim 21, Peng substantially discloses a clock generator (VCO 204) for outputting the test clock (SCK-1) 222. Peng does not explicitly disclose a test board on which a semiconductor integrated circuit device is removably mounted. However, Peng discloses a semiconductor die test jig 104, corresponding to a PCB test board, for holding and probing a semiconductor integrated circuit die or dice 202 having a test circuit, Figure 1 and 2. Furthermore, in analogous art, Conner discloses a printed circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuit, ICs, DUTs 116, for burn-in quality testing (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets as taught by Conner on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the

Art Unit: 2133

sockets during burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claims 22, 32, Peng substantially discloses the claimed invention as applied to claim 1, above. Peng does not explicitly disclose a frequency divider mounted on the test board for dividing the frequency of the test clock into a frequency, which can easily be measured. However, Peng discloses a modulo-N frequency divider 210 for dividing the clock output 222, located in the semiconductor integrated circuit die or dice 202, which is mounted on the semiconductor die test jig 104. Furthermore, in analogous art, Conner discloses a test fan out circuitry 214, which is mounted on a printed circuit board (PCB) Memory array board 210 (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount a test circuit, as taught by Conner, such as a modulo-N frequency divider 210 on the semiconductor die test jig 104 of Peng, for the purpose of performing test clock measurements at lower frequencies with respect to the operating frequency, since both Peng and Conner disclose standard testers that operate at low frequencies.

Regarding Claim 23, Peng substantially discloses a clock generator (VCO 204) for outputting the test clock (SCK-1) 222, wherein the two-pulse generator (burst controller 208) is fabricated in the semiconductor integrated circuit die or dice 202. Peng does not explicitly disclose a semiconductor integrated circuit device, which is removably mounted to a test board, and a clock generator mounted on the test board. However, Peng discloses a semiconductor integrated circuit die or dice 202, which is mounted on the semiconductor die test jig 104, and where the clock generator (VCO

Art Unit: 2133

204) is located in the semiconductor die test jig 104. Furthermore, in analogous art, Conner discloses a printed circuit board (PCB) Memory array board 210 having sockets for inserting integrated circuit, ICs, DUTs 116, for burn-in quality testing. The Memory array board 210 also includes a test fan out circuitry 214 that controls the provision of data from the devices under test 116 to error processor 124, (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount sockets and a test circuit, as taught by Conner, such as a VCO 204 on the semiconductor die test jig 104 of Peng for the purpose of inserting numerous memory chips into the sockets during burn-in quality testing, since sockets are well known in the art for providing flexibility, by removing or inserting chips during various testing stages. For example, following burn-in, the memory chips are generally removed from the burn in board and passed to a test stage where a more complete test is performed. Further motivation in using a test board with sockets is a result of some manufacturing operations, where memory devices are inserted into a burn-in board and the same board could be used for burn in and for holding memory devices for test, where the memory devices are passed directly from the burn-in stage to the test stage on the same printed circuit boards, and then memory devices are removed for final packaging upon completion of testing, thus reducing the number of transfer steps that are required during the semiconductor manufacturing operation, which can increase throughput and reduce cost (Col. 9, lines 57-67, Conner).

Regarding Claim 24, Peng discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by $1/N$ (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2. Wherein, the PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Regarding Claim 30, Peng substantially discloses a PLL circuit (phase-lock-loop) formed by the VCO 204, frequency divider 210 and phase detector 206 for synchronizing the frequency and phase of the internal clock output 222 to the frequency and phase of TCK 110, and using the modulo-N frequency divider 210 for dividing the clock output 222 frequency by a divide ratio N and then supplying the test clock output 222 to the two-pulse generator (burst controller 208). It is noted that dividing the clock output 222 by N is the equivalent of multiplying the clock output 222 by $1/N$ (col. 5, lines 51-62). The PLL circuit (phase-lock-loop) is fabricated in the semiconductor integrated circuit device (die or dice 202) Figure 2.

Peng does not explicitly disclose a second PLL circuit mounted on the test board.

Art Unit: 2133

However, in analogous art, Conner discloses a test fan out circuitry 214, which is mounted on a printed circuit board (PCB) Memory array board 210 (Figure 2, Conner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to mount a test circuit, as taught by Conner, such as a second PLL circuit on the semiconductor die test jig 104 of Peng, for the purpose of generating a clock at lower frequencies with respect to the operating frequency, since both Peng and Conner disclose standard testers that operate at low frequencies.

Response to Arguments

Applicant's arguments with respect to claims 1-4, 21-24, 30 and 32 have been considered but are moot in view of the new grounds of rejection.

Regarding independent Claim 1, in response to Applicant's argument, the Examiner notes that Jaber does not disclose or suggest a two-pulse generator for generating a two-pulse signal for scan path testing. However, under new grounds of rejection, Peng discloses a two-pulse generator (burst controller 208) for generating two clock pulses (310a and 310b) spaced from each other by a pulse interval equal to a period of a test clock (SCK-1) 222, as indicted in the present Office Action, above.

Art Unit: 2133

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 272-3824
Email: james.kerveros@uspto.gov

Date: 13 May 2005
Office Action: Non-Final Rejection

JAMES C KERVEROS
Examiner
Art Unit 2133

By:  5/13/05